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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHARLES RAY JOHNS, JAMES ALLAN KAHLE, PEICHUN PETER LIU, and THUONG QUANG TRUONG

Appeal 2008-004882
Application 10/809,553[1]
Technology Center 2100

Decided[2]: June 15, 2009

Before JAY P. LUCAS, JOHN A. JEFFERY, and STEPHEN C. SIU, *Administrative Patent Judges.*

LUCAS, *Administrative Patent Judge.*

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[1] Application filed March 25, 2004. The real party in interest is International Business Machines Corporation.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail date (paper delivery) or Notification Date (electronic Delivery).

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 1-21 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a direct memory access system with a tightly coupled arrangement of a cache, controller, and processor that makes software applications run faster. (*See* Spec. 2, ll. 3-7 and 5, ll. 12-14.) Appellants' claimed direct memory access controller executes commands for fetching data from a direct memory access cache and transferring the data to a local memory. (Spec. 5, ll. 4-14.) Data retrieval speeds of Appellants' invention are said to compare favorably with systems in which a controller fetches data from a common or system memory. (*Id.*) In the words of the Appellants:

> The present invention provides a system to provide software program control of cache management. The system comprises a processor . . . configured to generate direct memory access (DMA) commands for the management of a cache on the execution of a software program on the processor. The system further comprises a DMA controller . . . coupled to the processor that is configured to execute the DMA commands for the management of a cache.

(App. Br. 3) (internal citations omitted.)

Claims 1 and 2 are exemplary:

> 1. A system to provide software program control of cache management, comprising:

> a processor configured to generate DMA commands for the management of a cache on the execution of a software program on the processor; and
>
> a DMA controller coupled to the processor, configured to execute the DMA commands for the management of a cache.
>
> 2. The system of Claim 1, further comprising a cache coupled to the DMA controller, the system configured for the execution of the DMA commands for the management of a cache on the DMA controller to manage the operation of the cache coupled to the DMA controller.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Ohba	US 6,427,201 B1	July 30, 2002
Liao et al.	US 6,681,296 B2	Jan. 20, 2004
Ollivier et al.	US 6,737,881 B1	May 18, 2004 (filed Jun. 9, 2000)
Futral et al.	US 2005/0033874 A1	Feb. 10, 2005 (filed Aug. 5, 2003)

REJECTIONS

The Examiner rejects the claims as follows:

R1: Claims 1, 3, 9, 11, and 15-17 stand rejected under 35 U.S.C. § 102(e) for being anticipated by Futral.

R2: Claims 2, 7, 8, 10, 13, 14, 20, and 21 stand rejected under 35 U.S.C. § 103(a) for being obvious over Futral in view of Ollivier.

R3: Claims 4, 5, 12, 18, and 19 stand rejected under 35 U.S.C. § 103(a) for being obvious over Futral in view of Liao.

R4: Claim 6 stands rejected under 35 U.S.C. § 103(a) for being obvious over Futral in view of Ohba.

Groups of Claims:

Claims will be discussed in the order of the rejections, with the first claim in each rejection being representative, unless otherwise indicated. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants contend that the claimed subject matter is not anticipated by Futral, or rendered obvious by Futral in combination with any of Ollivier, Liao, or Ohba. The Examiner contends that each of the four groups of claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this opinion. Arguments that Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

We affirm-in-part.

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. §§ 102(e) and 103(a). The first issue

turns on whether Futral's direct memory access engine and processor anticipate Appellants' claimed "DMA controller" and "processor." The second issue is whether Ollivier's FIFO buffers, which temporarily store first inputted data being sent out to a destination port, render obvious Appellants' claimed "cache," which stores data that may be recalled frequently.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a system and method for generating and executing direct memory access commands. (*See* Spec. 2:14-20.) The system includes a processor coupled to a direct memory access controller. (*See* Spec. 4:11-13 and Fig. 1.) At least one embodiment of the claimed system includes a cache. (*See* claim 2.) However, other embodiments do not require a cache. (*See* claim 1 and Spec. 6:18-19.) The direct memory access controller may "retrieve" the same data from the cache when the cache is implemented in the system. (*See* Spec. 5:4-7.)

2. The Futral reference discloses a direct memory access engine 122 coupled to a processor 102. (*See* Fig. 1 and ¶¶ [0013], [0014].)

3. The Ollivier reference discloses a direct memory access system that includes a plurality of FIFO buffers. (*See* Fig. 3A; col. 5, ll. 40-48; and col. 6, ll. 53-57.) Ollivier's FIFO buffers (fifo 0 to fifo 6 in Fig. 3A) temporarily store data being sent by the direct memory access controller. (*See* Ans. 5; Ollivier, col. 5, ll. 11-12, 40-48.) No data is retrieved from

Ollivier's FIFO buffers for repeated use. (*See* Ollivier, col. 5, ll. 11-12, 40-48; col. 6, ll. 53-57.)

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

The intended use of a machine is not germane to the issue of patentability of the machine itself. *In re Casey*, 370 F.2d 576, 580 (CCPA 1967). There is an extensive body of precedent on the question of whether a statement in a claim of purpose or intended use constitutes a limitation for purposes of patentability. *See generally Kropa v. Robie*, 187 F.2d 150, 155-59 (CCPA 1951) (note the authority cited therein, and cases compiled in 3 Donald S. Chisum, *Chisum on Patents* § 8.06[1][d] (2008)). Such statements often, although not necessarily, appear in the claim's preamble. *In re Stencel*, 828 F.2d 751, 754 (Fed. Cir. 1987). However, the structure must be capable of performing the intended use.

"Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) (internal citations omitted). "In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is

anticipated, regardless of whether it also covers subject matter not in the prior art." *Id.*

ANALYSIS

From our review of the administrative record, we find that the Examiner has presented a prima facie case for the rejections of Appellants' claims under 35 U.S.C. §§ 102 and 103. The prima facie case is presented on pages 3 to 8 of the Examiner's Answer. In opposition, Appellants present a number of arguments.

Arguments with respect to the rejection of claims 1, 3, 9, 11, and 15-17 under 35 U.S.C. § 102 [R1]

Regarding exemplary claim 1, Appellants argue that Futral fails to teach a cache. (App. Br. 6.)

Specifically, Appellants argue: "The cited portions of *Futral* fail to teach or suggest DMA commands for the management of a cache. In fact, the word 'cache' does not appear anywhere in the *Futral* reference." (*Id.*)

We begin the analysis by noting that the "intended use" of a machine is not germane to the issue of patentability of a machine itself. *Casey*, 370 F.2d at 580. We have carefully reviewed exemplary claim 1, and indeed all of the claims, as well as the reference Futral. We find that the claim limitation "for the management of a cache" does not positively recite a cache, in that a cache is not established as a structural element of the system where claim 1 only recites "for the management of a cache." The claim limitation "for the management of a cache" is only an intended use of the claimed processor and the claimed controller without the cache being

brought into the body of the claim. As such language is mere intended use, *see Casey,* 370 F.2d at 580, the limitation "for the management of a cache" does not patentably distinguish over the cited prior art so long as the processor and controller are capable of performing this intended use.

In this case, claim 1 contains two particular claim elements, "a processor configured to generate DMA commands for the management of a cache" and "a DMA controller coupled to the processor for the management of a cache." Therefore, the only elements of the system as recited in exemplary claim 1 are a processor and a controller, and not a cache. (FF#1.) Since a cache is not claimed as a structural element of claim 1, Appellants' arguments are ineffective. (App. Br. 6.)

Appellants further argue that the Examiner improperly equated Futral's memory 116 with the cache recited in exemplary claim 1. (App. Br. 7.)

Specifically, Appellants argue: "It would be clear to a person of ordinary skill in the art that memory 116 of *Futral* is a slower storage and not a cache. If memory 116 were a cache, then *Futral* would call it a 'cache.'" (*Id.*)

As we stated above, Appellants failed to claim a cache where claim 1 recites the limitation "for management of a cache." That is, the limitation fails to establish a cache as a structural element of exemplary claim 1. Thus, it follows logically that whatever element of the Futral reference the Examiner cited as anticipating Appellants' cache is not relevant. The salient question is not whether Futral's memory 116 is a slower storage, as argued above by Appellants; instead, it is whether Appellants have even claimed a cache. We find that Appellants have not claimed a cache in exemplary

claim 1. Since Appellants' argument is centered on a limitation (*i.e.*, a "cache") not positively recited in exemplary claim 1, the argument is unpersuasive.

Appellants further argue that Futral fails to teach a DMA controller configured to execute DMA commands for cache management. (App. Br. 7.)

The Examiner points out in the Examiner's Answer that Appellants' DMA controller reads on Futral's DMA engine. (Ans. 9.) However, Appellants further contend that Futral cannot "possibly teach special DMA commands to be executed by a DMA controller for the management of a cache," since Futral fails to mention a cache. (Reply Br. 3.) We find no error in equating Futral's teaching of a DMA engine with the claimed DMA controller, as indeed Appellants' claimed DMA controller reads on Futral's DMA engine. Moreover, Appellants' argument concerning a cache is ineffective because, as we stated above, a cache has not been positively recited in exemplary claim 1. Accordingly, we are not persuaded of error in the Examiner's analysis.

The Examiner cited Futral for its processor (Appellants' processor) and DMA engine (Appellants' controller), which anticipate all of the elements (*i.e.*, the claimed processor and the claimed controller) of exemplary claim 1. In view of the reasoning expressed above for the application of the teachings of Futral, we are not persuaded of error in the rejection R1.

Arguments with respect to the rejection of claims 2, 7, 8, 10, 13, 14, 20, and 21 under 35 U.S.C. § 103 [R2]

Regarding exemplary claim 2, Appellants argue that Ollivier fails to disclose or suggest "a cache or a DMA controller configured to execute DMA commands for cache management." (App. Br. 8.)

The Examiner points out that Ollivier's Fig. 3A shows a plurality of FIFO (first-in, first-out) buffers. (*See* ref. nos. 310-315.) The Examiner collectively interprets Ollivier's FIFOs as being similar to Appellants' claimed "cache" as recited in exemplary claim 2. (*See* Ans. 5; Ollivier, Fig. 3A, ref. nos. 310-315.) We have carefully reviewed Appellants' arguments, as well as the Examiner's findings. We agree with Appellants' arguments.

We have studied Ollivier at the cited sections, and indeed the entire reference. We note that buffers, such as those shown in Ollivier's Figure 3A, are often used for temporarily storing data being transmitted from a first location to a second location, *see* Ollivier, column 5, lines 44 to 48, whereas caches are typically used for storing data that may be recalled from a single location, thereby saving repeated retrievals from typically slower main memory. In this case, Appellants' DMA controller may repeatedly recall the same data from the cache. (FF#1.) We construe exemplary claim 2 as requiring Appellants' claimed cache to store data, which may be available for repeated usage. (*Id.*) Therefore, we agree with Appellants' view, in that Ollivier's FIFO buffers would not have suggested Appellants' claimed "cache." To a person of ordinary skill in the computer arts, a buffer and a cache would not have been recognized as synonymous features. Ollivier's FIFO buffers do not operate similarly to Appellants' cache, since Ollivier's

FIFO buffers temporarily store burst data being sent from a source port to a destination port. (FF#1, FF#3.) Although the same burst data may be sent to Ollivier's FIFO buffers, the burst data is not stored in those buffers for purposes of recall to the source port. That is, no data is retrieved from Ollivier's FIFO buffers for repeated use, as FIFO buffers, by their nature, deliver out the "next inputted" data on a subsequent read. (FF#3.) We thus do not find support for the cache as claimed. It is to be noted that Futral also shows buffers (*see* Fig. 1, reference no. 126), but the Examiner declined to cite them in the rejection and thus did not refer to them as cache.

In view of this omission, we find that the Examiner erred in applying this rejection R2.

Arguments with respect to the rejection of claims 4, 5, 12, 18, and 19 under 35 U.S.C. § 103 [R3]

Appellants contend in their own words that "the *Liao* reference fails to teach or suggest providing DMA commands for cache management or a DMA controller that is configured to execute DMA commands for cache management." (App. Br. 9) (Appellants' emphasis.)

The Examiner points out in the Answer that Futral, and not Liao, is relied upon for disclosing the argued limitations. (Ans. 10-11.) Appellants contend that since Futral fails to mention a cache, Futral cannot "possibly teach special DMA commands to be executed by a DMA controller for the management of a cache." (Reply Br.) As we stated above, Appellants did not claim a cache in exemplary claim 1 on which claims 4 and 5 depend. Nor did Appellants claim a cache in either of independent claims 9 or 15

from which claims 12, 18, and 19 depend. Both claims 9 and 15 merely recite the limitation "for management of a cache" similar to exemplary claim 1. Since a cache was not claimed in any of the independent claims from which claims 4, 5, 12, 18, and 19 depend, Appellants' argument is ineffective. Accordingly, we find no error with the Examiner's analysis.

Arguments with respect to the rejection of claims 6 under 35 U.S.C. § 103 [R4]

Regarding claim 6, which stands or falls with exemplary claim 1, Appellants contend that "the Ohba reference fails to teach or suggest providing DMA commands for cache management or a DMA controller that is configured to execute DMA commands for cache management." (App. Br. 10) (Appellants' emphasis.)

The Examiner points out in the Answer that Futral, and not Ohba, is relied upon for disclosing the argued limitations. (Ans. 11.) We note that Appellants conceded in the opening Brief that Ohba "does appear to teach a DMA-tag command," the only element from Ohba that the Examiner relies on to reject claim 6.

Appellants further contend that since Futral fails to mention a cache, Futral cannot "possibly teach special DMA commands to be executed by a DMA controller for the management of a cache." (Reply Br. 3, top.) As we stated above, the claim limitation "for the management of a cache" is only an intended use of the claimed processor and the claimed controller without the cache being brought into the body of exemplary claim 1. Since a cache

was not claimed in claim 1, Appellants' argument is ineffective. Accordingly, we find no error with the Examiner's analysis.

CONCLUSION OF LAW

Based on the Findings of Facts and analysis above, we conclude that the Examiner erred in rejecting claims 2, 7, 8, 10, 13, 14, 20, and 21 under 35 U.S.C. § 103, as specified in R2. We did not find error in the rejection of all of the other claims in R1, R3, or R4.

DECISION

We decide as follows:

R1: The rejection of claims 1, 3, 9, 11, 15, 16, and 17 under 35 U.S.C. § 102(e) for being anticipated by Futral is Affirmed.

R2: The rejection of claims 2, 7, 8, 10, 13, 14, 20, and 21 under 35 U.S.C. § 103(a) for being obvious over Futral in view of Ollivier is Reversed.

R3: The rejection of claims 4, 5, 12, 18, and 19 under 35 U.S.C. § 103(a) for being obvious over Futral in view of Liao is Affirmed.

R4: The rejection of claim 6 under 35 U.S.C. § 103(a) for being obvious over Futral in view of Ohba is Affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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